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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,990	03/13/2000	Mou-Shiung Lin	085027-0026	6138

89518 7590 10/24/2011

McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005-3096

EXAMINER	
WALSH, DANIEL I	

ART UNIT	PAPER NUMBER
2887	

NOTIFICATION DATE	DELIVERY MODE
10/24/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com
SIP_Docket@mwe.com

Office Action Summary	Application No.	Applicant(s)	
	09/523,990	LIN ET AL.	
	Examiner	Art Unit	
	DANIEL WALSH	2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *44,48,49 and 60-68* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *44,48,49 and 60-68* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 44, 61, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coico et al. (US 6278193) in view of Miyaguchi et al. (US 5528825) and Hiromasa (JP362169448).

Coico et al. teaches a substrate (FIG. 1b and 22), a semiconductor chip (12) over a top surface of said substrate, wherein said semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface wherein the chip has

multiple pads at the front surface (FIG. 1a and 1b), multiple metal bumps between the pads of the chip and the top surface of said substrate (FIG. 1a-1b, as the chip pads 10 are electrically connected to the substrate pads 16 by solder reflow, thermo compression, or conductive adhesives). Accordingly, the use of metal bumps would have been an obvious expedient to produce the expected results of electrical connectivity. Alternatively, as the substrate pads are formed on top of the substrate, the pads themselves can broadly be interpreted as metal bumps/contacts.

Coico et al. is silent to an identity of product directly on said back surface of said semiconductor chip and an optically transparent layer vertically over said identity of product.

Miyaguchi et al. teaches that barcodes can be printed directly onto each IC 10 or on the package (col 3 lines 6+).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Coico et al. with those of Miyaguchi et al.

One would have been motivated to do this to provide a cost effective means for identification of a chip.

Coico et al./Miyaguchi et al. are silent to an optically transparent layer over top the identity of product.

Hiromasa teaches such limitations (abstract and constitution).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Coico/Miyaguchi et al. with those of Hiromasa.

One would have been motivated to do this for the expected results of wear resistance. Though Hiromasa teaches a package of an IC, as discussed above, the barcode can be printed on

a package or on the chip directly. Further, application of a resin layer over a printed barcode, provides the expected results of protection of the identifying information from wear.

The Examiner has intended such recited limitations in the product claims such as "identity of product information" as issues of printed matter/intended use that are not functionally related to the substrate. Accordingly, such non functional descriptive material doesn't patentably distinguish the claims from prior art with different types of printed/identifying information/marks, etc., as they are all alternative means/printed/marked of providing information (see In re Gulack/Ngai). This also applies to the "identity of manufacturer" and "barcode" for claims 61, 65, and their dependents.

Though explicitly silent to "identity of manufacturer" and "identity of product" the Examiner notes that the use of barcodes to convey information such as product information and manufacturer information is well known and conventional in the art as an obvious expedient to provide information related to a product. The type of information related to a product (product or manufacturer) is an issue of printed matter as discussed above.

2. Claims 48-49, 60, 62-64, and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coico et al./Miyaguchi et al./Hiromasa, as discussed above, in view of Flip Chip, as discussed in the previous Office Action.

Re claims 48-49, Coico et al./Miyaguchi et al./Hiromasa are silent to underfill and multiple balls. However, Coico et al. teaches the use of flip chips (col 1, liens 21+ and 45+) and how Coico et al. is directed to assist in their placement.

Flip Chip teaches flip chips with a BGA (page 1-2), including underfill between the substrate and chip and around the metal bumps/contacts, and multiple balls on the bottom surface of the substrate.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Coico et al./Miyaguchi et al./Hiromasa with those of Flip Chip.

One would have been motivated to do this in order to have a well known and conventional means to package a flip chip for low cost and reliability, increased performance, size, etc..

Re claim 60, the solder has been discussed above (see sole figure of Flip Chip).

Re claims 61 and 65, the limitations have been discussed above, wherein the Examiner notes that the type of printed matter/identification information on the chip is a matter of printed matter/intended use not functionally related to the substrate thereon, and therefore is not patentably distinct form the prior art which teaches markings on the substrate as discussed above.

Alternatively, since the claims and specification do not specifically recite or preclude such an interpretation, the Examiner notes that an identity of manufacturer could be identified from the alignment markings, or from the arrangement of the chip/substrate itself, from the barcode, etc. and such an interpretation is not preclude by the claims or specification, since they do not recite that the identity is actually printed or formed on the chip, but merely that it is on the backside. Therefore, it would have been obvious to identity based on the backside of the component itself, by recognizing the chip and therefore its manufacturer.

Re claims 62-68, the limitations have been discussed above, wherein the type of printed matter/information provided is not patentably distinct over the prior art since it is not functionally related to the substrate and is a matter of intended used.

3. Claims 44, 61, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coico et al. (US 6278193) in view of Hikita et al. (US 5528825), and Hiromasa (JP362169448).

Coico et al. teaches a substrate (FIG. 1b and 22), a semiconductor chip (12) over a top surface of said substrate, wherein said semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface wherein the chip has multiple pads at the front surface (FIG. 1a and 1b), multiple metal bumps between the pads of the chip and the top surface of said substrate (FIG. 1a-1b, as the chip pads 10 are electrically connected to the substrate pads 16 by solder reflow, thermo compression, or conductive adhesives). Accordingly, the use of metal bumps would have been an obvious expedient to produce the expected results of electrical connectivity. Alternatively, as the substrate pads are formed on top of the substrate, the pads themselves can broadly be interpreted as metal bumps/contacts.

Coico et al. is silent to an identity of product directly on said back surface of said semiconductor chip and an optically transparent layer vertically over said identity of product.

Hikita et al. teaches that barcodes can be printed directly onto each IC 10 or on the package (FIG. 15).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Coico et al. with those of Miyaguchi et al.

One would have been motivated to do this to provide a cost effective means for identification of a chip.

Coico et al./Hikita et al. are silent to an optically transparent layer over top the identity of product.

Hiromasa teaches such limitations (abstract and constitution).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Coico/Hikita et al. with those of Hiromasa.

One would have been motivated to do this for the expected results of wear resistance. Though Hiromasa teaches a package of an IC, as discussed above, the barcode can be printed on a package or on the chip directly. Further, application of a resin layer over a printed barcode, provides the expected results of protection of the identifying information from wear.

The Examiner has intended such recited limitations in the product claims such as "identity of product information" as issues of printed matter/intended use that are not functionally related to the substrate. Accordingly, such non functional descriptive material doesn't patentably distinguish the claims from prior art with different types of printed/identifying information/marks, etc., as they are all alternative means/printed/marked of providing information (see In re Gulack/Ngai). This also applies to the "identity of manufacturer" and "barcode" for claims 61, 65, and their dependents.

Though explicitly silent to "identity of manufacturer", as Hikita et al. teaches model designation, production lot number, and barcodes, the Examiner notes that the inclusion of identity of manufacturer, would have been an obvious expedient, as an issue of printed matter, to

provide relevant production information, and would have been well within the ordinary skill in the art to produce expected results.

4. Claims 48-49, 60, 62-64, and 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coico et al./Hikita et al./Hiromasa, as discussed above, in view of Flip Chip, as discussed in the previous Office Action.

Re claims 48-49, Coico et al./Hikita et al./Hiromasa are silent to underfill and multiple balls. However, Coico et al. teaches the use of flip chips (col 1, liens 21+ and 45+) and how Coico et al. is directed to assist in their placement.

Flip Chip teaches flip chips with a BGA (page 1-2), including underfill between the substrate and chip and around the metal bumps/contacts, and multiple balls on the bottom surface of the substrate.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the teachings of Coico et al./Hikita et al./Hiromasa with those of Flip Chip.

One would have been motivated to do this in order to have a well known and conventional means to package a flip chip for low cost and reliability, increased performance, size, etc..

Re claim 60, the solder has been discussed above (see sole figure of Flip Chip).

Re claims 61 and 65, the limitations have been discussed above, wherein the Examiner notes that the type of printed matter/identification information on the chip is a matter of printed matter/intended use not functionally related to the substrate thereon, and therefore is not patentably distinct form the prior art which teaches markings on the substrate as discussed above.

Alternatively, since the claims and specification do not specifically recite or preclude such an interpretation, the Examiner notes that an identity of manufacturer could be identified from the alignment markings, or from the arrangement of the chip/substrate itself, from the barcode, etc. and such an interpretation is not preclude by the claims or specification, since they do not recite that the identity is actually printed or formed on the chip, but merely that it is on the backside. Therefore, it would have been obvious to identity based on the backside of the component itself, by recognizing the chip and therefore its manufacturer.

Re claims 62-68, the limitations have been discussed above, wherein the type of printed matter/information provided is not patentably distinct over the prior art since it is not functionally related to the substrate and is a matter of intended used.

Response to Arguments

5. Applicant's arguments with respect to the rejection(s) of claim(s) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the art above.

6. The Examiner has applied the art of Coico et al. which teaches the structure of the chip, substrate, balls/pads, with the prior art of Miyaguchi et al./Hikita et al. which teaches barcodes printed on chips, along with Hiromasa which teaches a clear transparent resin over printed chip identification information for wear resistance.

Additional Remarks

7. In light of the lengthy prosecution for the current Application, the Examiner notes that recitations of a method for forming the circuit component, including a specific process and order of steps, in addition to reciting that the chip is/remains unpackagaged, and how the information read through the layer is used as part of the method, might help overcome the application of such prior art of teachings of flip chip/BGA devices being combined with barcode identification, and protection layers, if such claim amendments overcame the prior art.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ehrichs et al. (US 6593168) teaches a circuit component comprising a substrate (18), a semiconductor chip (10) over a top surface of said substrate, wherein said semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface, wherein said semiconductor chip comprises multiple pads (20) at said front surface, markings on said front surface of said semiconductor chip (alignment marks, FIG. 1-2), multiple bumps (20) between said multiple pads of said semiconductor chip and said top surface of said substrate. The Examiner notes that (col 5, lines 42+) teaches that the alignment marks can be formed during previous processing steps such that the marks are covered and visible through insulating layer 13, but Ehrichs et al. is silent to the markings/identity of product being visible through an optically transparent layer and wherein the identity of product is directly on the back surface of the chip, instead of the front.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WALSH whose telephone number is (571)272-2409. The examiner can normally be reached on M-F 9am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Paik can be reached on 571-272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DANIEL WALSH/
Primary Examiner, Art Unit 2887